Listing of Claims:

1. (Original) A method of responding to a read request in a system memory having a responding memory hub and at least one interposing memory hub through which a read response is transmitted on a data path of the interposing memory hub, the method comprising:

retrieving read data from a memory device coupled to the responding memory hub and preparing a read response including the read data;

generating an arbitration packet including data indicative of a data path configuration for the read response;

providing the arbitration packet and the read response to the interposing memory hub, the arbitration packet provided prior to the read response; and

receiving the arbitration packet at the interposing memory hub, decoding the data of the arbitration packet and enabling a data path for the read response in the interposing memory hub in accordance with the data of the arbitration packet.

2. (Original) The method of claim 1 wherein generating an arbitration packet comprises generating data for the arbitration packet that is used to distinguish the arbitration packet from a read response.

3. (Original) The method of claim 1 wherein generating an arbitration packet comprising generating a plurality of 8-bit bytes, the plurality of 8-bit bytes including one byte including data used by the interposing memory hub to distinguish the arbitration packet from a read response.

4. (Original) The method of claim 1 wherein enabling the data path for the read response comprises enabling a bypass data path in the interposing memory hub to couple the arbitration packet and read response through the interposing memory hub.

5. (Original) The method of claim 1, further comprising:

determining whether the interposing memory hub is busy; and

in the event that the interposing memory hub is not busy, generating the arbitration packet for provision to the interposing memory hub prior to providing the associated read response to the interposing memory hub.

6. (Original) The method of claim 1, further comprising:

determining whether a local data path of the responding memory hub is idle;

in the event that the local data path is idle, generating the arbitration packet for provision to the interposing memory hub prior to providing the associated read response to the interposing memory hub.

7. (Original) The method of claim 1 wherein generating the arbitration packet comprises generating an arbitration packet including data indicative of enabling a bypass data path in the interposing memory hub for coupling the arbitration packet and read response through the interposing memory hub.

8. (Original) A method of transmitting a read response on a data path of a memory hub interposed between a transmitting memory hub and a receiving memory hub, the method comprising:

receiving at the memory hub an arbitration packet including data indicative of a data path configuration for an associated read response;

decoding the arbitration packet;

configuring the data path in accordance with the data of the arbitration packet;

receiving the associated read response at the memory hub; and

coupling the associated read response to the configured data path for transmitting the same to the receiving memory hub.

9. (Original) The method of claim 8 wherein configuring the data path comprises enabling a bypass data path in the memory hub to couple the arbitration packet and read response through the memory hub to the receiving memory hub.

10. (Original) The method of claim 8, further comprising coupling the arbitration packet to the configured data path for transmitting the same to the receiving memory hub prior to transmitting the associated read response.

11. (Original) The method of claim 8, further comprising receiving a query from the transmitting hub whether the memory hub is busy and responding to the query by indicating to the transmitting hub that the memory hub is not busy.

12. (Original) A method of configuring a data path of a memory hub through which a read response is provided, the method comprising:

generating at a first memory hub an arbitration packet including data indicative of a data path configuration for an associated read response;

providing the arbitration packet to a second memory hub coupled to the first memory hub;

decoding the arbitration packet at the second memory hub; and

configuring a data path of the second memory hub in accordance with the data of the arbitration packet in preparation of receiving the associated read response.

13. (Original) The method of claim 12 wherein generating an arbitration packet comprises generating data for the arbitration packet that is used to distinguish the arbitration packet from a read response.

14. (Original) The method of claim 12 wherein configuring the data path comprises enabling a bypass data path in the second memory hub to couple the arbitration packet and read response through the second memory hub.

15. (Original) The method of claim 12, further comprising:

determining whether the second memory hub is busy; and

in the event that the second memory hub is not busy, providing the arbitration packet to the second memory hub prior to providing the associated read response to the second memory hub.

16. (Original) The method of claim 12, further comprising:

determining whether a local data path is idle;

in the event that the local data path is idle, generating the arbitration packet for provision to the second memory hub prior to providing the associated read response to the second memory hub.

17. (Original) The method of claim 12 wherein generating the arbitration packet comprises generating an arbitration packet including data indicative of enabling a bypass data path in the second memory hub for coupling the arbitration packet and read response through the second memory hub.

18. (Original) A method of communicating between a first and second memory hub for configuring a data path in the second memory hub, the method comprising:

generating an arbitration packet for an associated read response to be coupled through the second memory hub, the arbitration packet having a command code field including data identifying that it is an arbitration packet and further having a data path field including data indicative of a data path configuration in the second memory hub;

transmitting the arbitration packet prior to transmitting the associated read response to the second memory hub; and

configuring the data path in the second memory hub in accordance with the data included in the data path field.

19. (Original) The method of claim 18 wherein configuring the data path comprises enabling a bypass data path in the second memory hub to couple the arbitration packet and the associated read response through the second memory hub.

20. (Original) The method of claim 18, further comprising:

determining whether the second memory hub is busy; and

in the event that the second memory hub is not busy, generating the arbitration packet for provision to the second memory hub prior to providing the associated read response to the second memory hub.

21. (Original) The method of claim 19, further comprising:

determining whether a local data path is idle;

in the event that the local data path is idle, generating the arbitration packet for provision to the second memory hub prior to providing the associated read response to the second memory hub.

22. (Original) A memory hub coupled to at least one memory device, the memory hub comprising:

remote and local input nodes;

an output node;

a configurable data path coupled to the remote and local input nodes and further coupled to the output node, the configurable data path operable to couple at least one of a read response coupled through the remote and local input nodes to the output node; and

an arbitration control circuit coupled to the configurable data path, the output node, and the remote input node, the arbitration control circuit operable to generate an arbitration packet for an associated read response coupled through the local input node, the arbitration packet including data indicative of a data path configuration for the associated read response, the arbitration control circuit further operable to configure the configurable data path in accordance with the data included with an arbitration packet coupled thorough the remote input node in preparation of coupling an associated read response coupled through the remote input node to the output node.

23. (Original) The memory hub of claim 22 wherein the configurable data path comprises:

a multiplexer having an output coupled to the output node and a control node coupled to the arbitration control circuit;

a bypass data path coupled to the remote input node and a first input of the multiplexer;

a local queue having an input coupled to the local input node and further having an output coupled to a second input of the multiplexer; and

a remote queue having an input coupled to the remote input node and further having an output coupled to a third input of the multiplexer, the arbitration control circuit operable to generate a control signal for the multiplexer to selectively couple the bypass data path, local queue, or remote queue to the output node.

24. (Original) The memory hub of claim 22 wherein the arbitration control logic is further operable to generate data for the arbitration packet that is used to distinguish the arbitration packet from an associated read response.

25. (Original) A memory hub, comprising:

a bypass data path coupled between an input node and an output node on which read responses are coupled therebetween in response to being enabled; and

an arbitration control circuit coupled to the bypass data path operable to generate an arbitration packet in response to retrieving read data from a memory device coupled to the memory hub, the arbitration packet having a data path field including activation data to enable a bypass data path of an upstream memory hub, the arbitration control circuit further operable to receive an arbitration packet from a downstream memory hub and enable the bypass data path to couple a read response received therefrom from the input node to the output node.

26. (Original) The memory hub of claim 25, further comprising:

a multiplexer having an output coupled to the output node and a control node coupled to the arbitration control circuit, the multiplexer further having a first input coupled to the bypass data path;

a local queue having an input coupled to a local input node and further having an output coupled to a second input of the multiplexer; and

a remote queue having an input coupled to the input node and further having an output coupled to a third input of the multiplexer, the arbitration control circuit operable to generate a control signal for the multiplexer to selectively couple the bypass data path, local queue, or remote queue to the output node.

27. (Original) A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the memory devices through a memory device bus to access the memory devices, the memory hub comprising:

remote and local input nodes, the local input node coupled to the memory device bus;

an output node;

a configurable data path coupled to the remote and local input nodes and further coupled to the output node, the configurable data path operable to couple at least one of a read response coupled through the remote and local input nodes to the output node; and

an arbitration control circuit coupled to the configurable data path, the output node, and the remote input node, the arbitration control circuit operable to generate an arbitration packet for an associated read response coupled through the local input node, the arbitration packet including data indicative of a data path configuration for the associated read response, the arbitration control circuit further operable to configure the configurable data path in accordance with the data included with an arbitration packet coupled thorough the remote input node in preparation of coupling an associated read response coupled through the remote input node to the output node.

28. (Original) The memory module of claim 27 wherein the configurable data path of the memory hub comprises:

a multiplexer having an output coupled to the output node and a control node coupled to the arbitration control circuit;

a bypass data path coupled to the remote input node and a first input of the multiplexer;

a local queue having an input coupled to the local input node and further having an output coupled to a second input of the multiplexer; and

a remote queue having an input coupled to the remote input node and further having an output coupled to a third input of the multiplexer, the arbitration control circuit operable to generate a control signal for the multiplexer to selectively couple the bypass data path, local queue, or remote queue to the output node.

29. (Original) The memory module of claim 27 wherein the arbitration control logic of the memory hub is further operable to generate data for the arbitration packet that is used to distinguish the arbitration packet from an associated read response.

30. (Original) A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the memory devices through a memory device bus to access the memory devices, the memory hub comprising:

a bypass data path coupled between an input node and an output node on which read responses are coupled therebetween in response to being enabled; and

an arbitration control circuit coupled to the bypass data path operable to generate an arbitration packet in response to retrieving read data from a memory device coupled to the memory hub, the arbitration packet having a data path field including activation data to enable a bypass data path of an upstream memory hub, the arbitration control circuit further operable to receive an arbitration packet from a downstream memory hub and enable the bypass data path to couple a read response received therefrom from the input node to the output node.

31. (Original) The memory module of claim 30 wherein the memory hub further comprises:

a multiplexer having an output coupled to the output node and a control node coupled to the arbitration control circuit, the multiplexer further having a first input coupled to the bypass data path;

a local queue having an input coupled to a local input node and further having an output coupled to a second input of the multiplexer; and

a remote queue having an input coupled to the input node and further having an output coupled to a third input of the multiplexer, the arbitration control circuit operable to generate a control signal for the multiplexer to selectively couple the bypass data path, local queue, or remote queue to the output node.

32. (Original) A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a peripheral device port, the system controller further comprising a controller coupled to a system memory port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller;

a memory bus coupled to the system controller for transmitting memory requests and responses thereon; and

a plurality of memory modules coupled to the memory bus, each of the modules having:

a plurality of memory devices; and

a memory hub coupled to the memory devices through a memory device bus to access the memory devices, the memory hub comprising:

remote and local input nodes, the local input node coupled to the memory device bus;

an output node;

a configurable data path coupled to the remote and local input nodes and further coupled to the output node, the configurable data path operable to couple at least one of a read response coupled through the remote and local input nodes to the output node; and

an arbitration control circuit coupled to the configurable data path, the output node, and the remote input node, the arbitration control circuit operable to generate an arbitration packet for an associated read response coupled through the local input node, the arbitration packet including data indicative of a data path configuration for the associated read response, the arbitration control circuit further operable to configure the configurable data path in accordance with the data included with an arbitration packet coupled thorough the remote input node in preparation of coupling an associated read response coupled through the remote input node to the output node.

33. (Original) The processor-based system of claim 32 wherein the configurable data path of the memory hub comprises:

a multiplexer having an output coupled to the output node and a control node coupled to the arbitration control circuit;

a bypass data path coupled to the remote input node and a first input of the multiplexer;

a local queue having an input coupled to the local input node and further having an output coupled to a second input of the multiplexer; and

a remote queue having an input coupled to the remote input node and further having an output coupled to a third input of the multiplexer, the arbitration control circuit operable to generate a control signal for the multiplexer to selectively couple the bypass data path, local queue, or remote queue to the output node.

34. (Original) The processor-based system of claim 32 wherein the arbitration control logic of the memory hub is further operable to generate data for the arbitration packet that is used to distinguish the arbitration packet from an associated read response.

35. (Original) A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a peripheral device port, the system controller further comprising a controller coupled to a system memory port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller;

a memory bus coupled to the system controller for transmitting memory requests and responses thereon; and

a plurality of memory modules coupled to the memory bus, each of the modules having:

a plurality of memory devices; and

a memory hub coupled to the memory devices through a memory device bus to access the memory devices, the memory hub comprising:

a bypass data path coupled between an input node and an output node on which read responses are coupled therebetween in response to being enabled; and

an arbitration control circuit coupled to the bypass data path operable to generate an arbitration packet in response to retrieving read data from a memory device coupled to the memory hub, the arbitration packet having a data path field including activation data to enable a bypass data path of an upstream memory hub, the arbitration control circuit further operable to

receive an arbitration packet from a downstream memory hub and enable the bypass data path to couple a read response received therefrom from the input node to the output node.

36. (Original) The processor-based system of claim 35 wherein the memory hub further comprises:

a multiplexer having an output coupled to the output node and a control node coupled to the arbitration control circuit, the multiplexer further having a first input coupled to the bypass data path;

a local queue having an input coupled to a local input node and further having an output coupled to a second input of the multiplexer; and

a remote queue having an input coupled to the input node and further having an output coupled to a third input of the multiplexer, the arbitration control circuit operable to generate a control signal for the multiplexer to selectively couple the bypass data path, local queue, or remote queue to the output node.